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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,954	06/27/2003	Kenichi Osada	500.38532CX1	8677

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,954	OSADA ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *2,8-13,15 and 17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,14,16 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/565,535.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/27/03,8/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Applicant's election with traverse of the embodiment of figures 10-12 in the reply filed on 8/10/2004 is acknowledged. The traversal is on the ground(s) that claim 1 is generic, and thus claims 2-7 and 14-18 should be allowed upon the allowance of claim 1. This is not found persuasive because claim 6 is independent claim, which includes limitations which are not disclosed in the embodiment of figures 10-12. However, dependent claims 2-7 and 14-15 would be allowed upon the allowance of claim 1.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> **The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.**

1. Claims 1, 3-7, 14, 16 and 18 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the embodiment of figures 4-5 for an outer shape of the diffusion layer defined by an isolation layer extending along the entirety of each of the longitudinal sides of the diffusion layer, as recited in claim 1, and for first and second switch, as recited I claim 16.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-5, 7, 14, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara et al. (5,930,163) in view of Minami et al. (5,072,286). Regarding claims 1 and 16, Hara et al. teach in figure 1 and related text (column 5, line 58 to column 6, line 65) an SRAM memory device comprising first and second inverters including first N type MOS transistor TN1 with first P type MOS transistor TP1 and second N type MOS transistor TN2 with second P type MOS transistor TP2, respectively, with an input terminal of the second inverter is connected to the output terminal of the first inverter and the input terminal of the first inverter being connected to the output terminal of the second inverter (figure 16 and column 8, lines 30-34), third and fourth N type MOS transistors TN3, TN4 having sources connected to the output terminals of the first and second inverters, respectively, and drains connected to first and second bit lines, respectively, and also gates connected to word lines, wherein

TN1 and TN3, are respectively formed in a first P type well region, wherein

TN2 and TN4 are formed in a second P type well region,

wherein TP1, TP2 are formed in an N type well which lies between first and second P type well regions, and

wherein the first P type well region includes a diffusion layer wherein an outer shape of the diffusion layer ND1 (the rectangular shaded area) is substantially linearly

symmetric relative to a line extending in a first direction through the first P type well region, and wherein the boundary of the first P-type well region and the N-type well region extends in the first direction (column 4, lines 53-57 and column 6, lines 39-45). Hara et al. do not teach in figure 1 an isolation layer extending along the entirety of each of the longitudinal sides of the diffusion layer.

Minami et al. teach in figures 4 and 6B an isolation layer 101, 102 extending along the entirety of each of the longitudinal sides of the diffusion layer 25.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an isolation layer extending along the entirety of each of the longitudinal sides of the diffusion layer in Hara et al.'s device in order to provide better electrical isolation to the diffusion layer. Note that forming an isolation layer along the entirety of each of the longitudinal sides of the diffusion layer in Hara et al.'s device does not prevent from the additional diffusion region to be formed adjacent to diffusion layer ND1, below the surface of the semiconductor substrate.

Regarding claim 3, Hara et al. teach in figure 1 an outer shape of the diffusion layer ND1 in the first P type well being a combination of rectangles having identical widths, rendering them indistinguishable from each other, and thus combined to a rectangle having even sides.

Regarding claims 4, 5 and 7, Hara et al. teach in figure 2 first and second bit lines BL lie between a first power supply line Vdd and first and second ground lines GND (upper and lower ground lines), respectively, and first and second ground lines are coupled to the sources of the TN1 and TN2, respectively (figure 16), wherein a first bit line, first power supply line and first and second ground lines are formed metal layers having the

same level at the same metalization level (figure 2 and column 5, line 66 to column 6, line 1), and wherein the first word line lies in a metalization level between the substrate and the first and second bit lines.

Regarding claim 14, Hara et al. teach in figure 1 and related text (column 3, lines 54-65) a first polycrystalline silicon lead layer for use as the gate of the third N-channel MOS transistor TN3 and a second polycrystalline silicon lead layer for use as the gate of the first P-channel MOS transistor TP1 and also as the gate of the first N-channel MOS transistor are disposed in parallel to each other (figure 2 and column 6, lines 12-18), wherein a third polycrystalline silicon lead layer for use as the gate of the fourth N-channel MOS transistor TN2 and a fourth polycrystalline silicon lead layer for use as the gate of the second N-channel MOS transistor and also as the gate of the second P-channel MOS transistor TP2 are disposed in parallel to each other, and wherein the first and third polycrystalline silicon lead layers are connected via a contact to a second layer of a metal lead layer constituting the first word line.

Regarding claim 18, prior art teaches wherein the diffusion layer formed in said N-type well region or P-type region has its planar shape of a combined form as resulting from combination of a first rectangle having long sides in the elongate direction of boundary lines of said N-type well region and said first and second P-type well regions along with a short side of a first length and a second rectangle having long sides in the elongate direction of the boundary lines of said N-type well region and said first and second P-type well regions along with a short side of a second length, the combination being in the elongate direction of said boundary lines.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
9/16/04

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800